WEST Search History

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DATE: Wednesday, October 20, 2004

Hide?	Set Name	Query	Hit Count
		DB=USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR	
☐	L5	L3 same (set$4 near4 mode near4 operation)	15
☐	L4	L3 same (set$4 near4 mode)	71
☐	L3	L2 same (execut$4 near2 (command or instruction))	744
☐	L2	L1 with mode	5851
☐	L1	(command or instruction) near2 (data or information)	123685

END OF SEARCH HISTORY

L5: Entry 1 of 15 File: USPT Jun 27, 2000

DOCUMENT-IDENTIFIER: US 6081687 A
TITLE: Copying machine provided with an image reading apparatus for scanning moving documents

Detailed Description Text (98):
The data inputted through interrupt communication from each CPU are analyzed (step S63), and according to the analysis, operation mode setting is conducted (step S64). When command setting is performed (step S65), commands to execute the operation modes set in step S64 are created, and the command data are set in an output area for outputting through communication (step S66). Then, other necessary processes are finally performed (step S67).

L5: Entry 2 of 15 File: USPT Mar 28, 2000

DOCUMENT-IDENTIFIER: US 6044157 A
TITLE: Microprocessor suitable for reproducing AV data while protecting the AV data from illegal copy and image information processing system using the microprocessor

Brief Summary Text (24):
With the above construction, it is possible to prevent an illegal action, where the AV data store instruction is executed without the AV data decompress instruction being executed, by setting a limitation of updating the operation mode to the first operation mode. This is because firstly, to execute the AV data store instruction independently, the operation should be the first operation mode, and secondly, the AV data reproduce instruction, which has no limitation on the operation mode, performs processes of loading and decompressing the AV data inseparably.

L5: Entry 5 of 15 File: USPT Jun 25, 1996

DOCUMENT-IDENTIFIER: US 5530804 A
TITLE: Superscalar processor with plural pipelined execution units each unit selectively having both normal and debug modes

Detailed Description Text (137):
The user and supervisor programming models displayed in FIGS. 4, 5, 6, and 7, along with the user and supervisor mode contents of the memory map shown in FIG. 3, comprise the operating environment of the data processor 10. The concept of a programmer's model is needed in order to completely understand the test/debug/emulation mode discussed herein which is an architectural extension. Operation in the debug/emulator/test mode will utilize the instruction set of the data processor, but access the separate "debug mode" address spaces in the memory map of FIG. 3, for most instructions executed in debug/emulator/test mode. There is one programming model set of registers, thus instructions executed in debug/emulator/test mode can read and manipulate the registers displayed in FIGS. 5, 6, and 7. Therefore, prior to operation in debug/emulator/test mode, register contents should be saved to memory 22 to capture their original user or supervisor mode contents prior to debug/emulator/test mode operation. By performing this memory store of the programmer's model, the state of the processor in normal mode just before entrance of the test/debug/emulation mode can be restored once the test/debug/emulation mode is exited. Therefore the test/debug/emulation mode discussed herein is non-obtrusive and non-destructive to normal operation.

L5: Entry 7 of 15 File: USPT May 9, 1995

DOCUMENT-IDENTIFIER: US 5414570 A
**** See image for Certificate of Correction ****
TITLE: Tape marks recorded in user data blocks having identifications of the recorded tape marks

Detailed Description Text (15):
The above described FIG. 12 illustrated mode set command 400 is preferably only in the same chain of commands in which the recording data transfer is to occur between the host and the recording device. Depending on the mode, the mode set command 400 can be in a chain of commands executed earlier than the data recording chain of commands. The term chain of commands is a known term and is also described briefly in the Bauer, et al., supra, and Videki U.S. Pat. No. 4,471,457, as well as in other documents. In another mode of operation, the mode set command 400 is used only during a chain of commands in which the data transfer occur. At the end of the command chain the autoblocking mode can be automatically reset within the control unit or a second mode set command may be issued by the host processor to disable the autoblocking, i.e., reset bit 90 for the device indicated in the mode set command. Power on reset also resets the autoblocking bit 91. By arbitrary protocol in the preferred embodiment, if a mode set command 400 is not received in the chain of commands for a write data transfers then the control unit will reset bit 91 for the device addressed by the chain of commands. The mode set to autoblocking enables the determination, based on record length, whether or not autoblocking is to be used, all as will become apparent.

L5: Entry 12 of 15 File: JPAB Sep 21, 1992

DOCUMENT-IDENTIFIER: JP 04264651 A
TITLE: PERIPHERAL CONTROLLER

Abstract Text (2):
CONSTITUTION: When an input/output instruction from the host device is received, a processing part 12 checks the command code. In the case of an instruction for setting the operation mode, the operation mode of a peripheral equipment 2 is set to that instructed from the host device. The level of the storage area of a storage device 11 is selected from information included in the flag field of the input/output instruction, and information on the operation mode is stored in the storage area of the level. When the host device outputs the input/output instruction except for the instruction indicating the setting of the operation mode, the processing part 12 selects the level of the storage area of the storage part 11 based on information on the flag field and reads information on the operation mode from the storage area of the level. The operation mode of the peripheral equipment 2 is set in accordance with having read information and an operation instructed by the command code is executed.